What is claimed is:

1. Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented each time an operation is executed by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation.

2. Processor according to claim 1, wherein the state unit has continuous states.

3. Processor according to claim 1, wherein the state unit is so designed that the state of the state unit is also a function of time.

4. Processor according to claim 1, wherein the state unit is so designed that, when the computation unit performs no operations, the state of the state unit changes in a direction which is opposite to the direction of change in response to execution of an operation.

5. Processor according to claim 1, wherein the state unit is so designed that the speed of the computation unit is inversely proportional to the variable, by which the state of the state unit can be represented.

6. Processor according to claim 1, wherein the state unit is so designed that the speed of the computation unit is in-

versely exponential to the variable, by which the state of the state unit can be represented.

7. Processor according to claim 1, wherein the state unit includes a capacitor and the state is a charge state of the capacitor.

8. Processor according claim 1, wherein the state unit includes a unit with a thermal capacitance and the state is a temperature of the unit.

9. Processor according to claim 8, wherein the unit with a thermal capacitance also has a second temperature and the speed of the computation unit can also be controlled according to the second temperature.

10. Processor according to claim 1, wherein a frequency of a clock rate of the computation unit can be controlled according to the state of the state unit.

11. Processor according to claim 1, wherein a number of bits which are processed by an operation in the computation unit can be controlled according to the state of the state unit.

12. Processor according to claim 1, wherein the operation is a cryptographic operation for encrypting or decrypting information.

13. Method for executing an operation in a processor at a variable speed, comprising the following steps:

increasing a variable which represents a state of a state unit by a specified value each time the operation is executed by a computation unit of the processor; and

decreasing the speed of the computation unit in response to the increase of the variable due to the execution of the operation.